REMARKS

This is intended as a full and complete response to the Office Action dated April 4, 2005, having a shortened statutory period for response set to expire on July 4, 2005. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-23 are pending in the application. Claims 11-15, 17 and 20-23 remain pending following entry of this response. Claims 11, 13 and 17 have been amended. Claims 1-10, 16, 18 and 19 have been cancelled. Applicants submit that the amendments do not introduce new matter.

Claim Objections

Claims 19 are objected to because of the duplicated numbered claims (i.e., two claims numbered 19). Both claims numbered 19 have been canceled.

Claim Rejections - 35 USC § 102

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by *Arimoto et al.* (U.S. Patent No. 6,744,684, hereinafter "*Arimoto*"). Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Arimoto* does not disclose "each and every element as set forth in the claim". For example, *Arimoto* does not disclose monitoring, by a memory controller, write operations to memory cells and maintaining a plurality of bits indicating rows of containing memory cells involved in monitored write operations, and transferring those bits to a memory device, or a system for doing the same, as claimed in claims 11 and 20, respectively. As another example, *Arimoto* does not disclose a memory device having row state circuitry configured to maintain a plurality of bits indicative of rows that

are to be refreshed, interface circuitry configured to receive the plurality of bits from a memory controller and to transfer the plurality of bits to the row state circuitry, and refresh enable circuitry configured to limit the number of rows for which refresh requests are issued based on the bits of the row state circuitry, as claimed in claim 13.

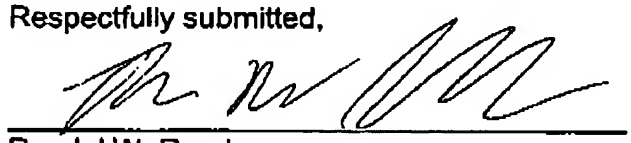
In fact, Applicant fails to find any teaching in *Arimoto* of maintaining a set of bits indicating rows containing memory cells that have been written to by any type device and certainly no teaching of limiting which rows are refreshed based on such bits. Further, while the Examiner states that a memory controller is shown in Figure 6 (reference number 40), Applicant submits reference number 40 is a command generation circuit (see col. 10, lines 54-63) which is internal to a DRAM core. Therefore, Applicant submits that *Arimoto* does not anticipate claims 11, 13, and 20.

Accordingly, Applicants submit claims 11, 13, and 20, as well as those claims that depend therefrom, are in condition for allowance.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted,



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